

FORM: PTO-1449
(REV: 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEAtty Docket No:
95-0653.01Serial No:
08/984,560

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(37 CFR 1.98(b))

(use several sheets if necessary)

Applicant:
Mailloux et al.Filing Date:
December 3, 1997Group:
2751

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
sh	AA	5,357,469	10/94	Sommer et al.	365	193
↑	AB	5,268,865	12/93	Takasugi	365	189.5
	AC	4,618,947	10/86	Tran et al.	365	230
	AD	5,267,200	11/93	Tobita	365	189.5
	AE	4,344,156	8/82	Eaton et al.	365	203
	AF	4,707,811	11/87	Takemae et al.	365	239
	AG	4,649,522	3/87	Kirsch	365	189
	AH	4,603,403	7/86	Toda	365	189
	AI	4,567,579	1/86	Patel et al.	365	189
↓	AJ	4,484,308	11/84	Lewandowski et al.	365	900
sh	AK	4,875,192	10/89	Matsumoto	365	193

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FOREIGN PATENT DOCUMENTS

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Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

sh	AR		Samsung Electronics, "Samsung Synchronous DRAM", March 1993, pgs. 1-16
ldh	AS		Oki Electric Ind. Co., Ltd., "Burst DRAM Function & Pinout", 2nd presentation, Item #619, September, 1994
sh	AT		Toshiba, "Pipelined Burst DRAM", December 1994, JEDEC JC-42.3 Hawaii

Examiner:

H. Kim

Date Considered:

9/12/99

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.



Sheet: 2 of :9

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Examiner Initial	Document Number	Date	Name	Class	Subclass	
RL	AA 4,685,089	8/87	Patel et al.	365	233	
	AB 4,562,555	12/85	Ouchi et al.	365	233	
	AC 4,575,825	3/86	Ozaki et al.	365	189	
	AD 4,788,667	11/88	Nakano	365	193	
	AE 5,392,239	2/95	Margulis et al.	365	189	
	AF 5,379,261	1/95	Jones, Jr.	365	230.01	
	AG 5,126,975	6/92	Handy et al.	365	230.01	
	AH 5,331,593	7/94	Merritt	365	189.11	
	AI 5,331,471	7/94	Matsumoto Gilbert	365	189.05	
	AJ 5,526,320	6/96	Zagar et al.	365	233.5	

FOREIGN PATENT DOCUMENTS

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OTHER ART (including author, title, date, pertinent pages, etc.)

AR		Toshiba America Electronic Components, Inc., "Application Specific DRAM, 1994", Pgs. C-178, C-260, C218
AS		Micron Semiconductor, Inc., "Synchronous DRAM 2 MEG x 8 SDRAM", Pgs. 2-3 through 2-6, Rev. 4/94
AT		Toshiba America Electronic Components, Inc., "4M DRAM 1991", Pgs. A-137 - A-159

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Examiner Initial	Document Number	Date	Name	Class	Subclass	
dh	AA 5,268,865	12/93	Takasugi	365	189.05	
	AB 5,319,759	6/94	Chan	365	230.08	
	AC 5,327,390	7/94	Takasugi	365	230.08	
	AD 5,426,606	6/95	Takai	365	230.06	
	AE 5,369,622	11/94	McLaury	365	233	
	AF 5,568,445	10/96	Park et al.	365	233	
	AG 5,652,724	7/97	Manning	365	189.05	
	AH 5,610,864	3/97	Manning	365	193	
	AI 5,526,320	6/96	Zagar et al.	365	233.5	
	AJ 5,392,239	2/95	Margulis et al.	365	189.01	
dh	AK 5,175,835	12/92	Beighe et al.	711	212	

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OTHER ART (including author, title, date, pertinent pages, etc.)

dh	AR		Micron Semiconductor, Inc., "1994 DRAM Data Book", pgs. 2-1 to 2-6
sh	AS		Mosel-Vitellic V53C8257H DRAM Specification Sheet, 20 pgs.
sh	AT		Toshiba Corp., "Integrated Circuit Technical Data-262,144 Words x 8 Bits Multiport DRAM", TC52826TS/Z/FT/TR, TEN. Rev. 2.1

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U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
Wk	AA 5,146,582	9/92	Begun	395	280	
	AB 4,851,990	7/89	Johnson et al.	395	280	
	AC 4,519,028	5/85	Olsen et al.	395	559	
	AD 5,652,724	7/97	Manning	365	189.05	
	AE 5,457,659	10/95	Schaefer	365	222	
	AF 5,452,261	9/95	Chung et al.	265	233	
	AG 5,280,594	1/94	Young et al.	395	425	RECEIVED
	AH 5,058,066	10/91	Yu	365	189.05	
	AI 4,870,622	9/89	Aria et al.	365	230.02	MAR 02 1999
	AJ 5,668,773	09/97	Zagar et al.	365	233	
Wk	AK 5,325,502	06/94	McLaury	395	425	Group 2700

FOREIGN PATENT DOCUMENTS

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OTHER ART (including author, title, date, pertinent pages, etc.)

Wk	AR		Micron Technology, Inc., "Burst EDO DRAM Information", pgs. 1-126, Rev. 9/95
Wk	AS		NEC "Command Truth Table" March 15, 1993
Wk	AT		Samsung Electronics "KM48SV2000 Preliminary CMOS SDRAM" Rev.1(Mar, 1993), pgs. 7-8

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b)) (use several sheets if necessary)		Applicant: Mailloux et al.	
		Filing Date: December 3, 1997	Group: 2751

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
Wk	AA 5,373,227	12/94	Keeth	323	313	
Wk	AB 5,410,670	04/95	Hansen et al.	395	425	
Wk	AC 5,349,566	09/94	Merritt et al.	365	233.5	
Wk	AD 5,682,354	10/97	Manning	365	233.5	
Wk	AE 5,640,364	06/97	Merritt et al.	365	233.5	
Wk	AF 5,729,504	12/95	Cowles	365	236	
Wk	AG 5,661,695	08/97	Zagar et al.	365	233.5	
Wk	AH 5,305,284	04/94	Iwase	365	238.5	
Wk	AI 5,325,330	06/94	Morgan	365	189.05	
Wk	AJ					
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OTHER ART (including author, title, date, pertinent pages, etc.)

Wk	AR		S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages
Wk	AS		Electronic News "Mitsubishi Samples 16M Synch DRAM", 10/25/93, pgs. 3-4
Wk	AT		"DRAM 1 Meg X 4 DRAM 5BEDO Page Mode", 1995 DRAM Data Book, pp.1-1 thru 1-30,, (Micron Technology, I)

Examiner: K. Kom	Date Considered: 9/12/99
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Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

sk	AR		"Hyper Page Mode DRAM", 8029 Electronic Engineering, 66, No. 813, Woolwich, London, GB, pp. 47-48, (September 1994)
gh	AS		Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)
pe	AT		Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode Access", IEEE, Cutsom Integrated Circuits Conference, pp. 781-786, (March 3, 1992)

Examiner:

H. Kim

Date Considered:

9/12/99

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Wh	AR		Micron Semiconductor, Inc., "Synchronous DRAM 4 Meg x 4 SDRAM", Pgs. 2-1 to 2-2
Wh	AS		Micron Technology, Inc., "1996 DRAM Data Book", Pgs. 1-1 to 1-52, and 4-1 to 4-42
Wh	AT		Micron Technology, Inc., "1995 DRAM Data Book", Pgs. 3-1 to 3-37

Examiner: H. Korn	Date Considered: 9/12/99
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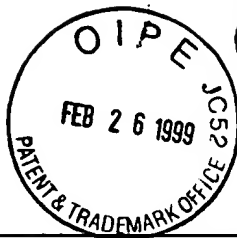
OTHER ART (including author, title, date, pertinent pages, etc.)

nlk	AR		Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)
	AS		Access", IEEE, Custom Integrated Circuits Conference, pp. 781-786, (March 3, 1992)
			S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages
Wh	AT		Micron Technology, Inc., "1995 DRAM Data Book" pp. 4-1 thru 4-42, 12/95.

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116	AR		"Rossini, Pentium, PCI-ISA, Chip Set", Symphony Laboratories, entire book, June 1995
	AS		
	AT		

Examiner:

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